PCI Express Controller

PRODUCT BRIEF

Overview

Highly Configurable
Technology Independent
System Validated

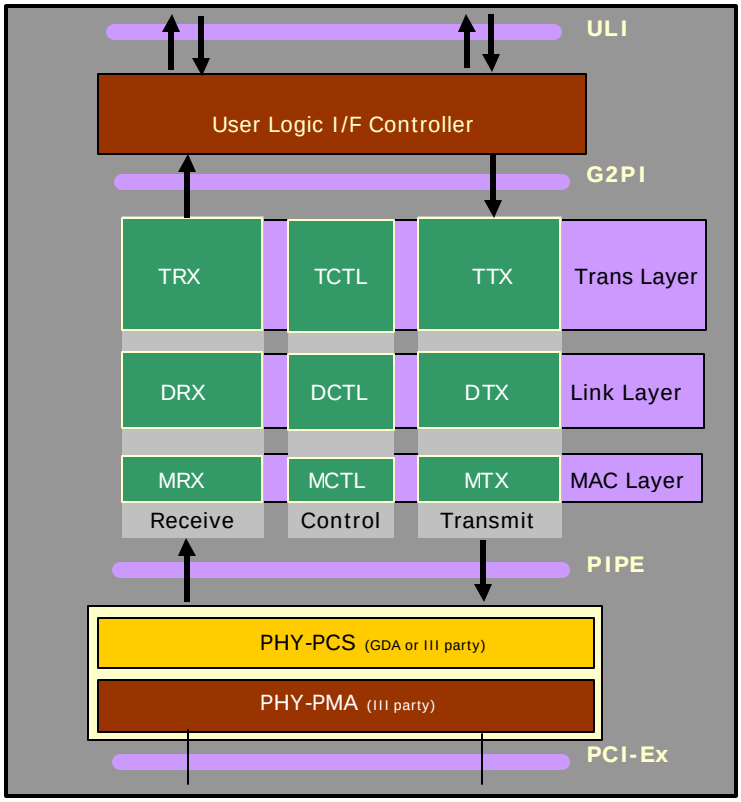
GDA's PCI Express interface controller is a highly flexible and configurable design targeted for end-point, root-complex, switch and bridge implementations in desktop, server, mobile, networking and telecom applications. The controller architecture is carefully tailored to optimize link utilization, latency, reliability, power consumption, and silicon footprint.

The controller's simple, configurable and layered architecture is independent of application logic, PHY designs, implementation tools and, most importantly, the target technology. GDA solution allows the licensees to easily migrate among FPGA, Gate array and Standard cell technologies optimally. Its flexible backend interface makes it easy to be integrated into wide range of applications. GDA solution provides highly scalable bandwidth through configurable lanes, widths and frequencies.

GDA's PCI-Express solution leverages years of experience in PCI, PCI-X and HyperTransport technologies and the expertise in creating system validated IP solutions with RTL, synthesis, simulation, board and software elements to offer lowest risk in terms of compliance and inter operability. GDA is the leading solution provider for HyperTransport, another high speed PCI-on-packets technology, with many licenses sold in compute and networking markets.

Features

- Compliant to PCI Express base specification version 1.0a
- Targets end-point, bridge, switch and root-complex solutions
- Implements transaction, data link and physical layers
- Supports multiple lanes: x1, x2, x4, x8 or x16
- Architected for high link utilization and low latency
- Efficient receive and transmit-retry buffering scheme
- Completely handles PCI-Express ordering rules
- Implements flow control logic for both directions
- Packet oriented user logic interface
- Supports PIPE based PHY architecture
- Optional DMA controller on the user logic side
- Flexible lane ordering and support for lane reversal



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Specifications

Configurable Options

- Maximum Link Width (x1, x2, x4, x8, x16)
- Maximum TLP data payload size supported (64B to 4KB)
- Transmit Retry/Receive Buffer size
- Number of Virtual Channels
- Upstream port / downstream port
- Inclusion of specific sublayers etc.

Design Attributes

- Highly modular and configurable design
- Layered architecture
- Fully synchronous design
- Supports both sync and async reset
- Clearly demarked clock domains
- Software control for key features
- Multiple loop backs for debug

Status	:	Under development
Availability	:	Q3, 2003
Language	:	Verilog, VHDL
Synthesis	:	Synopsys, Synplicity
Simulation	:	Cadence, Synopsys
Technology	:	FPGA, 0.18u ASIC or better

Product Package

- Configurable RTL Code
- HDL based test bench and behavioral models
- Test cases
- Protocol checkers, bus watchers and performance monitors
- Configurable synthesis shell

Documentation

- Design Guide
- Verification Guide
- Synthesis Guide

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