# PCI Express RC Port Controller

PRODUCT BRIEF

## Overview

### High Performance
### Highly Configurable
### Maximum offload

GPEX-RC is a highly flexible and configurable design targeted for root complex implementations in desktop, server and embedded applications. GPEX-RC is part of GDA's PCI-Express (GPEX) family of IP solutions which includes End Point (GPEX-EP) and Advanced Switching (GPEX-AS) designs.

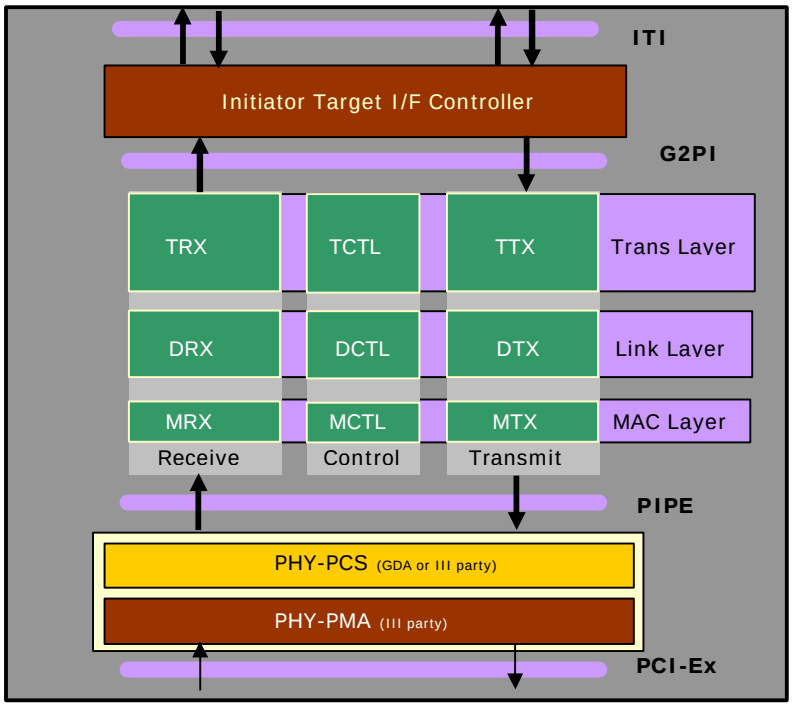
GPEX-RC controller architecture is carefully tailored to optimize the link utilization, latency, reliability, power consumption and silicon footprint. The design offers maximum offload through the hardware logic provided for configuration, interrupt, power management, error reporting, and message handling. The solution also offers high degree of dynamic programmability through a range of registers and a peripheral interface.

GPEX-RC's simple, configurable and layered architecture is independent of application logic, PHY designs, implementation tools and, most importantly, the target technology. This solution allows the licensees to easily migrate among FPGA, Gate array and Standard cell technologies optimally.

GPEX-RC leverages GDA's years of experience in PCI, PCI-X, Hyper Transport and PCI-Express technologies and the expertise in creating system validated IP solutions with RTL, synthesis, simulation, board and software elements to offer lowest risk in terms of compliance and interoperability. GDA is a leading IP provider for high-speed interconnect technologies, with several licenses sold in compute, storage and networking markets.

## Features

- Compliant to PCI-Express Specification, Rev 1.0a
- Complete port controller logic for Root Complex implementatio
- Implements transaction, data link and physical layers
- Supports multiple lanes: x1, x2, x4, x8 or x16
- Support multiple virtual channels: 1-8
- Implements a bridge config space and config generation logic
- Efficiently mapping of PCI-Express intr to local intr resources
- Hardware assisted power management scheme
- Message manager to map error messages to local events
- Efficient error management scheme
- Peripheral interface to access config and additional registers
- Flexible receive and transmit-retry buffering scheme
- Completely handles PCI-Express ordering rules
- Architectured for high link utilization and low latency
- Supports PIPE based PHY architecture





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# PCI Express RC Port Controller

| | | |
|---|---|---|
| Availability | : | Q104 |
| Language | : | Verilog HDL |
| Synthesis | : | Synopsys DC |
| Simulation | : | Verilog-XL/NC Verilog |
| Technology | : | 0.18u ASIC or better, FPGA |


| | | |
|---|---|---|
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## Specifications

### Configurable Options

- Maximum link width (x1, x2, x4, x8, x16)
- Maximum TLP data payload size supported (64B to 4KB)
- Transmit and Receive Retry buffer size
- Number of Virtual Channels
- Inclusion or exclusion of specific sub-layers
- Data path width 32/64/128
- Configuration space options

### Design Attributes

- DFT friendly, Fully synchronous design
- Layered Architecture
- Sync or Async Reset support
- Clearly demarked clock domains
- Software control for key features

### Product Package

- RTL view in Verilog HDL
- Comprehensive functional test bench
- Synthesis scripts
- Compliance checklist test suite
- Protocol checkers, bus watches and performance monitors
- Training and support programs

### Documentation

- Data Sheet
- Design Guide
- Verification Guide
- Synthesis Guide