GRIO: RapidIO Controller

PRODUCT BRIEF

Overview

High Performance
Technology Independent
System Validated

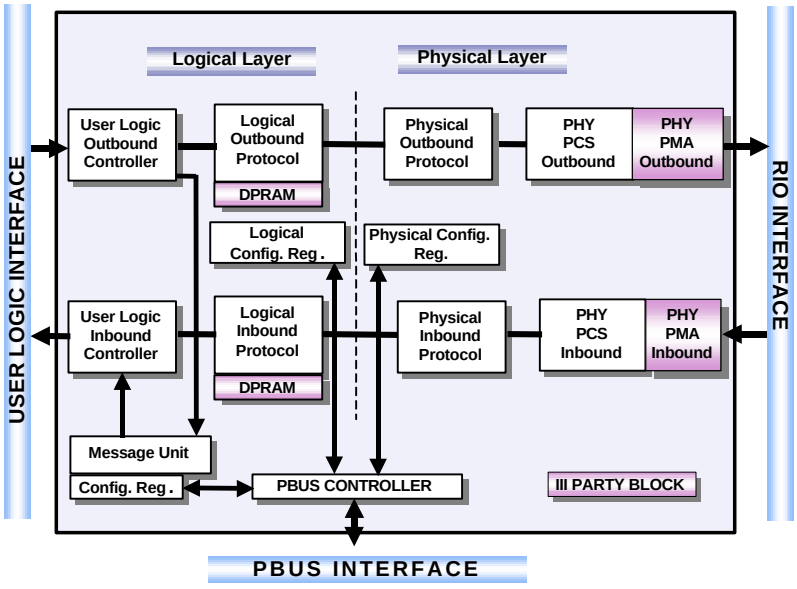
The RapidIO Interconnect Architecture, designed to be compatible with the most popular integrated communications processors, host processors, and networking digital signal processors, is a high-performance, packet-switched, interconnect technology. It addresses the high-performance embedded industry's need for reliability, increased bandwidth, and faster bus speeds in an intra-system interconnect. The RapidIO interconnect allows chip-to-chip and board-to-board communications at performance levels scaling to ten Gigabits per second and beyond.

GDA's RapidIO controller core (GRIO) is designed to meet the growing needs of the industry. The core's simple, configurable and layered architecture is independent of applications, PHY designs, implementation tools and, most importantly, the target technology. The hardware and software configurable features make the core suitable for use in multiple applications. The design targets embedded systems, telecommunication, networking and any application where high speed, low latency response, low pin counts, reliability and scalability are necessary.

GDA's RapidIO Controller solution leverages years of experience in PCI, PCI-X, HyperTransport and PCI Express technologies and the expertise in creating fully compliant, system validated, interoperable IP solutions with RTL, synthesis, simulation, board and software components. GDA is the leading solution provider for fast interconnect technologies like HyperTransport, PCI Express and 10G Ethernet with many licenses sold in the compute and networking markets.

Features

- Compliant with RapidIO specification, Revision 1.2
- Supports both Serial and Parallel interfaces
- Supports 1x and 4x serial interfaces at 1.25/2.5/3.125Gbps
- Supports 8 and 16 bit parallel interfaces at 250/375/500 MHz
- Implements physical, transport and logical layer functions
- Supports both input/output and message passing protocols
- Implements receiver controlled flow control
- Supports all transaction flows and priorities
- Support for up to 256 bytes data payload
- Supports 34 bit addressing
- Implements a flexible buffer management scheme
- Performs link initialization, training, error detection and recovery
- Performs auto detection of interface widths and modes
- Supports multi-cast event control symbols
- Targets FPGA, Structured ASIC and Standard Cell technologies



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Specifications

Configurable Options

- Serial, Parallel or both interfaces
- Inclusion of messaging unit
- Buffer sizes
- Interface widths, modes and line rates
- Inclusion of user logic interface controller

Availability : Q2 2004
Language : Verilog HDL
Synthesis : Synopsys/Synplify
Simulation : Verilog-XL, NC Verilog, VCS
Technology : 0.13u or better

Design Attributes

- Highly modular
- Fully synchronous
- Layered architecture
- Technology independent
- Scan friendly RTL
- Clearly demarked clock domains

Product Package

- RTL code
- Verification environment
- Test cases
- Synthesis environment
- Training and Support

Documentation

- Design guide
- Verification guide
- Synthesis guide

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