SPI4 Multi-Channel

PRODUCT BRIEF

Overview

Highly Configurable
System Validated
Wide Choice of PHY

SPI-4 Phase 2 is an interface defined for packet or cell transfer between physical layer device and link layer device, for aggregate bandwidth of OC-192 ATM, Packet over SONET/SDH, and 10 Gbps Ethernet applications.

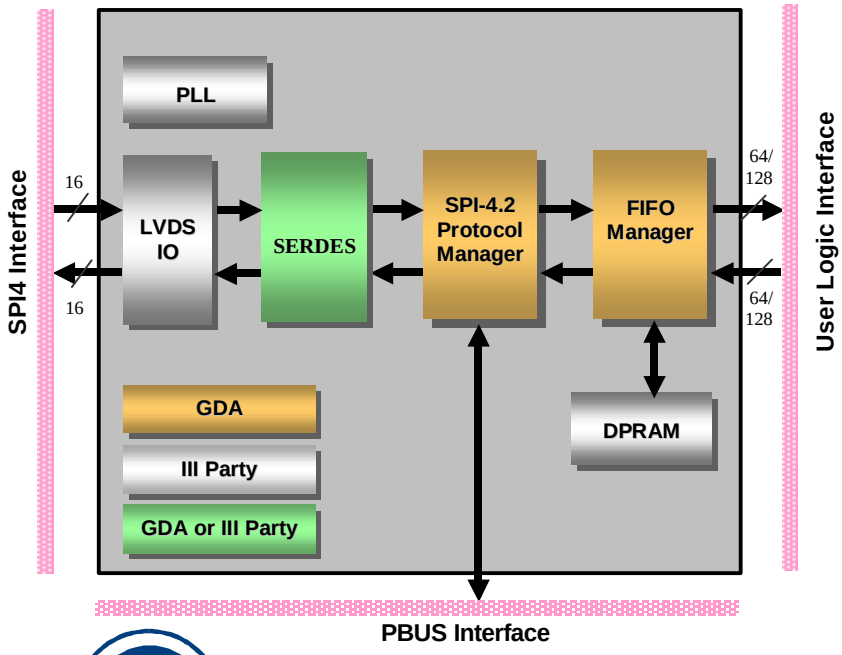
GDA's SPI4P2 Interface controller is a highly configurable and efficient implementation, fully compliant to Optical Internet working forum's OIF-SPI4-02.0, System packet level interface Level 4 Phase 2 implementation agreement. SPI4P2 is a fully digital, multi-module design created to provide complete solution in variety of application scenarios: from dynamic alignment through protocol and FIFO management.

The core's simple, configurable and layered architecture is independent of applications, PHY designs, implementation tools and, most importantly, target technologies. GDA's SPI4P2 Interface Controller is a cost-effective, end-to-end system validated solution that allows the licensees to easily migrate to FPGA, Gate array and Standard cell technologies optimally.

GDA's SPI4P2 solution, leverages years of experience in creating reusable designs for Ethernet, PCI Express, and HyperTransport technologies and the expertise in creating system validated solutions with RTL, synthesis, simulation, board and software elements to offer risk-free solution in terms of compliance and interoperability.

Features

- Compliant to OIF-SPI4-02.0, OIF's SPI-4.2 implementation agreement
- Modular structure with optional digital serdes and FIFO manager blocks.
- Supports 64 or 128 bit user logic interface.
- Supports single and multi link operations – scalable from 1 to 256 links
- Supports "LVTTL" or "LVDS" or "LVTTL&LVDS" signaling for status path.
- Supports micro level de-skew and bit level de-skew on the receive paths.
- Single user logic interface or multiple user logic interfaces.
- Interrupt generation for reserved control words, DIP4 error, SOP error, EOP error.
- Bandwidth optimized design using shared sop-eop control word without filling idle control words.
- Supports flexible FIFO schemes.



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SPI4 Multi-Channel

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Specifications

Configurable Options

- 64-bit or 128-bit internal data path.
- Configurable number of ports (1 to 256).
- IO status (LVTTL, LVDS, LVTTL+LVDS).
- Configurable FIFO depth.
- Configurable Maximum transmit and receive calendar length.
- Single user logic interface or multiple user logic interfaces.
- Synchronous or Asynchronous reset.
- Optional FIFO manager.

Design Attributes

- Fully synchronous design.
- Technology–independent design.
- Scan friendly and parameterized RTL code.
- Clearly demarked clock domains.
- Highly modular design: partitioned by function, timing, and testability.

Status	:	Gold [system validated]
Availability	:	Available
Language	:	Verilog HDL
Synthesis	:	Synopsys/Synplify
Simulation	:	Verilog-XL/NC Verilog/VCS
Technology	:	0.13u or better

Product Package

- Verilog RTL Code.
- Detailed design document.
- Automated and parameterized test bench
- Test cases.
- Synthesis environment.
- Training and Support.

Documentation

- Design guide.
- Verification guide
- Synthesis guide
- User guide.

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