



GDA USB2.0 Device Controller

PRODUCT BRIEF

Overview Features

Highly Configurable Technology Independent

GDA's USB 2.0 Device controller is a highly configurable core and implements the USB 2.0 device functionality. USB2.0 device controller core can be easily integrated with GDA's Pravega family of USB 3.0 cores for providing complete USB3.0 solution.

The USB2.0 Device Controller core can be configured to support control endpoint and any allowed number of Bulk, Isochronous and Interrupt endpoints. Control transfer processing can be supported natively by the core or optionally by an external processor.

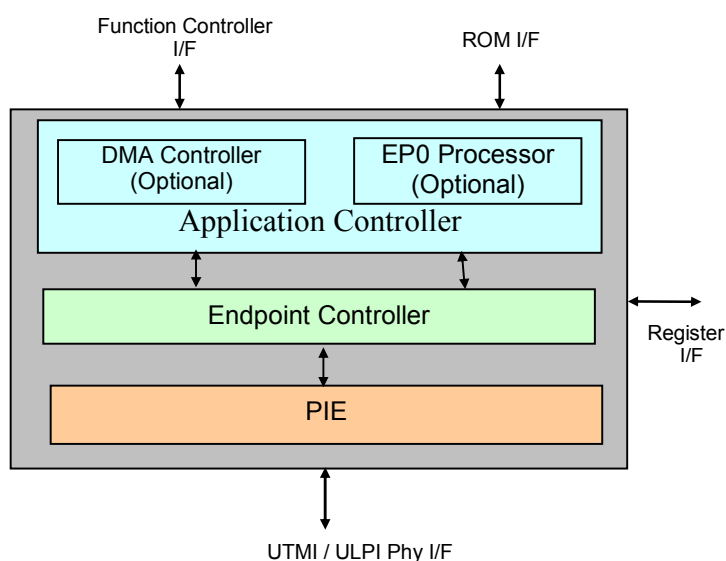
The USB2.0 Device Controller core is architected with a high performance DMA engine and application interface for maximizing performance. The USB 2.0 Device Controller core supports all defined USB 2.0 power states. The design is carefully partitioned to support standard power management schemes.

The USB 2.0 Device controller has UTMI / ULPI compliant physical layer interface and can be easily integrated with third party transceiver cores.

The controller has a very simple application interface which can be easily adapted to standard on-chip-bus interfaces such as AXI, AHB, OCP as well as other standard off-chip interconnects.

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- Compliant with USB2.0 Specification
- Supports High Speed and Full Speed
- Supports Interrupt/Bulk/Isochronous/Control Transfers
- Supports Suspend / Resume and Remote Wakeup.
- Configurable Application Frequency.
- Flexible User Application Logic which can be used by any SoC/OCP interface.
- User Application Logic has Optional DMA controller with configurable buffers sizes or Optional Standard FIFO Interface, in absence of DMA controller.
- User Application Logic has Optional Endpoint Zero Block for processing the Standard Device Descriptor
- Configurable Datapath on User Application Interface (32/64/128 bit)
- Supports UTMI or ULPI compliant Physical Layer interface
- Support for various Hardware and Software Configurability regarding Core characteristics.
- Configurable number of Configurations, Interfaces, Alternative Interfaces and endpoints.
- FPGA validated



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GDA USB2.0 Device Controller

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Specifications

Configurable Options

- Support of Hardware and Software Configurability
- Optionally supports FS operations
- Configurable number of Configurations, Interfaces, Alternative Interfaces and Endpoints
- Configurable Application Layer
 - Optional proprietary DMA Engine
 - Configurable depth for Tx and Rx FIFOs.
 - Optional EPO processor
- Configurable Endpoint Characteristics (Max Pkt Size, EP Direction, EP Type etc)

Design Attributes

- Highly modular and configurable design
- Layered architecture
- Fully synchronous design
- Supports both sync and async reset
- Clearly demarked clock domains
- Software control for key features

Product Package

- Configurable RTL Code
- HDL based test bench and behavioral models
- Test cases
- Protocol checkers, bus watchers and performance monitors
- Configurable synthesis shell

Documentation

- Design Guide
- Verification Guide
- Synthesis Guide

Status : **Bronze**

Availability : **Contact – ip@gdatech.com**

Language : **Verilog**

Synthesis : **Synopsys DC, Synplicity**

Simulation : **Cadence, Synopsys**

Technology : **130nm ASIC or better, FPGA**

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