



GDA USB3.0 Device Controller (Pravega – DC)

PRODUCT BRIEF

Overview Features

Highly Configurable Technology Independent

GDA's USB 3.0 Device controller is a highly configurable core and implements the USB 3.0 device functionality that can be interfaced with third party USB 3.0 PHY's. USB3.0 device controller core is part of USB3.0 family of cores named "Pravega". The core leverages GDA's design expertise from its high speed interconnect family of IP's including PCI Express, Serial RapidIO and Hypertransport.

The Pravega Device Controller core can be configured to support control endpoint and any allowed number of Bulk, Isochronous and Interrupt endpoints. Control transfer processing can be supported natively by the core or optionally by an external processor.

The Pravega Device Controller core is architected with a high performance DMA engine and application interface for maximizing performance of streaming data. The Pravega Device Controller core supports all defined USB 3.0 power states. The design is carefully partitioned to support standard power management schemes. Optionally, it can be configured to manage power mode transitions of the controller and the USB 3.0 PHY for aggressive power savings required for mobile and handheld devices.

The controller has a very simple application interface which can be easily adapted to standard on-chip-bus interfaces such as AXI, AHB, OCP as well as other standard off-chip interconnects.

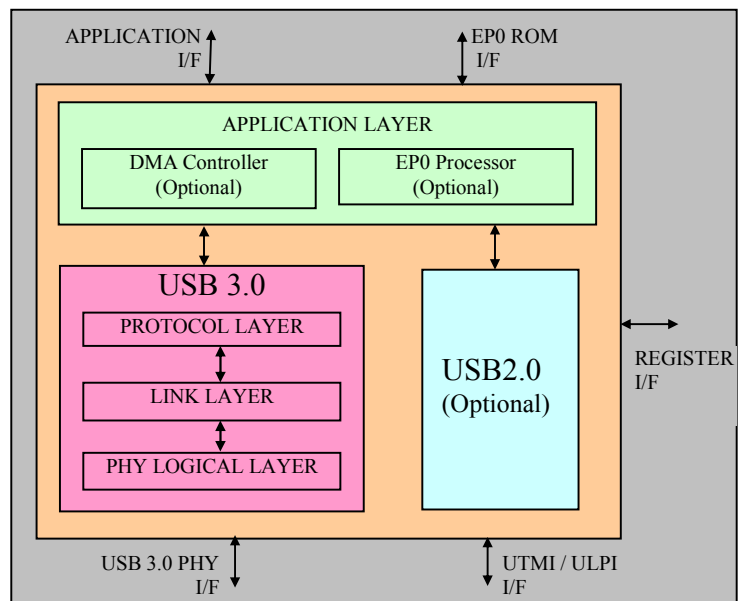
www.gdattech.com



K.K. Strategic Sourcing

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- Compliant with USB3.0 Specification Version 1.0
- Supports Interrupt /Bulk/Isochronous/Control Transfers
- LFPS Support
- Supports Aggressive Low Power Management
- Configurable Core Frequency.
- Flexible User Application Logic which can be used by any SoC/OCP interface.
- Flexible User Application Logic
 - Standard FIFO Interface or an Optional DMA controller
 - Can be adapted to any SoC / OCB interface.
 - Optional Endpoint Zero Block for processing the Standard Device Descriptor
- Configurable Datapath on User Application Interface : 32, 64, 128 bit
- Configurable USB 3.0 PIPE Interface: 8, 16, 32 bit.
- Support for various Hardware and Software Configurability regarding Core characteristics.
- Configurable number of Configurations, Interfaces, Alternative Interfaces and endpoints.



GDA Technologies, Inc.
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Specifications

Configurable Options

- Support of Hardware and Software Configurability
- Optional USB2.0 Core for Backward Compatibility
- Configurable number of Configurations, Interfaces, Alternative Interfaces and Endpoints
- Configurable Application Layer
 - Optional proprietary DMA Engine
 - Configurable depth for Tx and Rx DMA FIFOs.
 - Optional EP0 processor for processing control transfers.
- Configurable Endpoint Characteristics (Max Pkt Size, EP Direction, EP Type etc)

Design Attributes

- Highly modular and configurable design
- Layered architecture
- Fully synchronous design
- Supports both sync and async reset
- Clearly demarked clock domains
- Software control for key features
- Multiple loop backs for debug
- Extensive clock gating support
- Multiple Power Well Support

Product Package

- Configurable RTL Code
- HDL based test bench and behavioral models
- Test cases
- Protocol checkers, bus watchers and performance monitors
- Configurable synthesis shell

Documentation

- Design Guide
- Verification Guide
- Synthesis Guide

Status : **Bronze**
Availability : **Contact – ip@gdatech.com**
Language : **Verilog**
Synthesis : **Synopsys DC, Synplicity**
Simulation : **Cadence, Synopsys**
Technology : **130nm ASIC or better, FPGA**

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