GDA USB3.0 Host Controller (Pravega – HC)

PRODUCT BRIEF

Overview

Highly Configurable

Technology Independent

GDA's USB 3.0 Host controller is a highly configurable core and implements the USB 3.0 Host functionality that can be interfaced with third party USB 3.0 PHY's. USB3.0 Host controller core is part of USB3.0 family of cores named "Pravega". The core leverages GDA's design expertise from its high speed interconnect family of IP's including PCI Express, Serial RapidIO and Hypertransport.

The Pravega Host Controller core is architected with an optional high performance DMA engine based on xHCI specification. The core can be configured to support full fledged xHCI implementations for use in standard PCIe-USB bus adaptors/chip sets or be configured with a subset of features for embedded applications requiring limited host functionality.

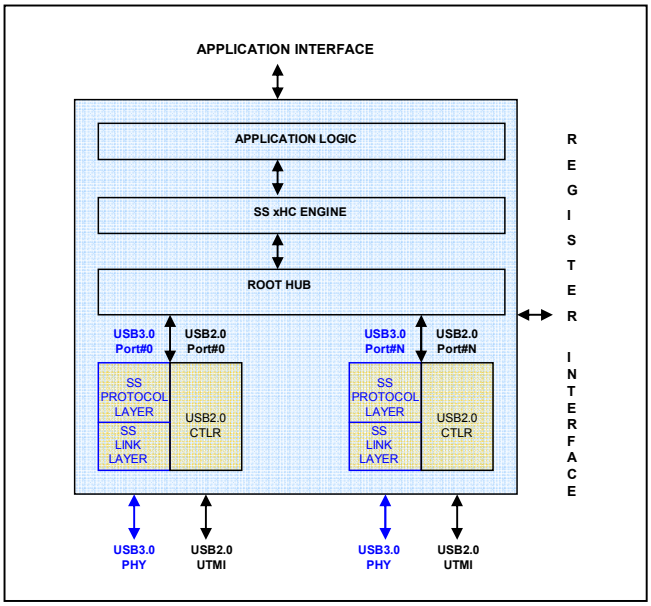
The Pravega Host Controller core is carefully partitioned to support standard power management schemes which include extensive clock gating and multiple power wells for aggressive power savings required for mobile and handheld applications.

The controller has a very simple application interface which can be easily adapted to standard on-chip-bus interfaces such as AXI, AHB, OCP as well as other standard off-chip interconnects making it easy to be integrated in a wide range of applications.

The controller's simple, configurable and modular architecture is independent of application logic, PHY designs, implementation tools and, most importantly, the target technology. GDA solution allows the licensees to easily migrate among FPGA, Gate array and Standard cell technologies optimally.

Features

- Compliant with xHCI Rev0.95
- Compliant with USB3.0 Specification Rev1.0
- Implements Phy Logical/ Link / Protocol Layers.
- Asynchronous clocking between Host Controller and Application logic
- Supports Aggressive Low Power Management
- Configurable core frequency: 125, 250, 500 Mhz.
- Configurable PIPE Interface: 8, 16, 32 bit.
- Optional Host Controller Engine
  - Support for normative optional features
  - Support for multi-port implementation
- Flexible User Application Logic
  - Can be adapted by any SoC / OCB interface / offchip interconnects
  - Configurable Datawidth: 32, 64, 128 bit.
- Simple Register Interface for internal Register Access.
- Support for various Hardware and Software Configurability regarding Core characteristics.



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GDA Technologies, Inc.
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GDA USB3.0 Host Controller (Pravega – HC)

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Status : **Bronze**
Availability : **Contact – ip@gdatech.com**
Language : **Verilog**
Synthesis : **Synopsys DC, Synplicity**
Simulation : **Cadence, Synopsys**
Technology : **130nm ASIC or better, FPGA**

Specifications

Configurable Options

- Optional USB2.0 Core for Backward Compatibility
- Application Interface – AHB, AXI, PCIe, Low Latency Pravega Native Packet Interface
- Configurable Buffer Sizes
- Optional xHCI Engine with configurable number of device slots, interrupters, root hub ports, configurable scratchpad support, optional support for host initiated stream data movement and optional debug capability etc

Design Attributes

- Highly modular and configurable design
- Layered architecture
- Fully synchronous design
- Supports both sync and async reset
- Clearly demarked clock domains
- Extensive clock gating support
- Multiple Power Well Support
- Software control for key features
- Multiple loop backs for debug

Product Package

- Configurable RTL Code
- HDL based test bench and behavioral models
- Test cases
- Protocol checkers, bus watchers and performance monitors
- Configurable synthesis shell

Documentation

- Design Guide
- Verification Guide
- Synthesis Guide

Mar 2008 Version 1.0

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