



GDA USB3.0 Hub Controller (Pravega – HubC)

PRODUCT BRIEF

Overview Features

Highly Configurable Technology Independent

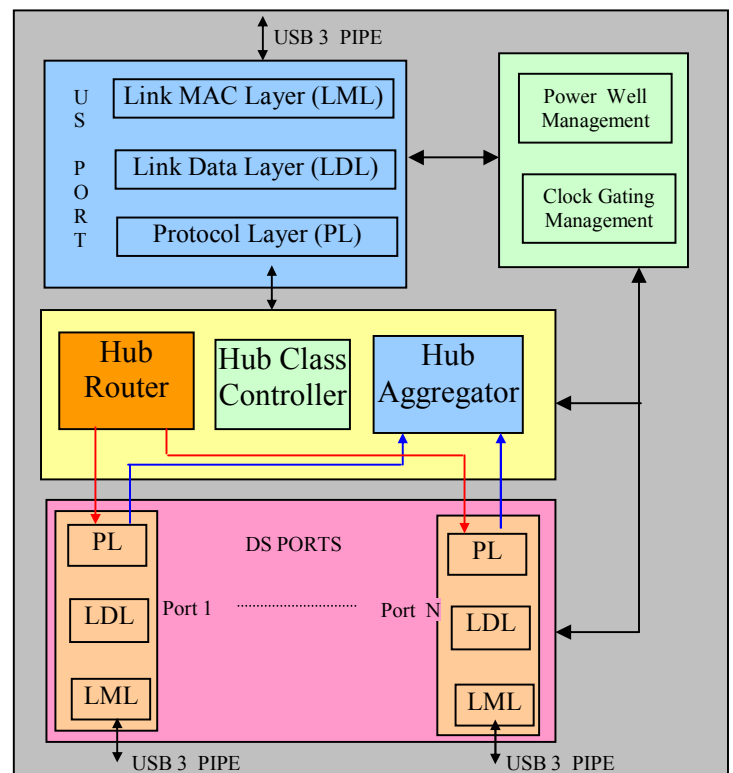
GDA's USB 3.0 Hub controller is a highly configurable core and implements the USB 3.0 Hub functionality that can be interfaced with third party USB 3.0 PHY's. USB3.0 Hub controller core is part of USB3.0 family of cores named "Pravega". The core leverages GDA's design expertise from its high speed interconnect family of IP's including PCI Express, Serial RapidIO and Hypertransport.

The Pravega Hub Controller core can be configured to support upto 15 downstream ports.

The Pravega Hub Controller core supports all defined USB 3.0 power states. The design is carefully partitioned to support standard power management schemes. Optionally, it can be configured to manage power mode transitions of the controller and the USB 3.0 PHY for aggressive power savings required for bus powered hubs.

The controller's simple, configurable and layered architecture is independent of application logic, PHY designs, implementation tools and, most importantly, the target technology. GDA solution allows the licensees to easily migrate among FPGA, Gate array and Standard cell technologies optimally. Its flexible backend interface makes it easy to be integrated into wide range of applications

- Compliant with USB3.0 Specification Version 1.0
- Configurable number of downstream ports
- Configurable Core Frequency
- Configurable Internal datapath width: 32, 64, or 128 bits
- Compliant with standard USB 3.0 PHY Interface
- Configurable PHY Interface width: 8, 16, or 32 bits
- Efficient buffering scheme for forwarding packets through hub with minimal latency
- Supports Bus and Self Powered Hub implementations
- USB 3.0 low power states support
- Extensive clock gating and multiple power well support for aggressive power savings
- Support for various Hardware and Software Configurability regarding Core characteristics
- Register Interface for internal Register Access
- Optional Support for USB2.0 Hub controller



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Specifications

Configurable Options

- Support of Hardware and Software Configurability
- Optional USB2.0 Hub Controller
- Configurable Buffer sizes
- Configurable shared buffers or per port buffers
- Configurable number of Downstream Ports

Design Attributes

- Highly modular and configurable design
- Layered architecture
- Fully synchronous design
- Supports both sync and async reset
- Clearly demarked clock domains
- Software control for key features
- Multiple loop backs for debug
- Extensive clock gating support
- Multiple Power Well Support

Status : Bronze

Availability : Contact – ip@gdatech.com

Language : Verilog

Synthesis : Synopsys DC, Synplicity

Simulation : Cadence, Synopsys

Technology : 130nm ASIC or better, FPGA

Product Package

- Configurable RTL Code
- HDL based test bench and behavioral models
- Test cases
- Protocol checkers, bus watchers and performance monitors
- Configurable synthesis shell

Documentation

- Design Guide
- Verification Guide
- Synthesis Guide

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